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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,517	06/26/2003	Charles Seelcy	P2002,0542	1168

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LERNER AND GREENBERG, P.A.
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EXAMINER	
CONTINO, PAUL F	
ART UNIT	**PAPER NUMBER**
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/607,517	SEELEY ET AL.	
	Examiner	Art Unit	
	Paul Contino	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION: Non-Final Rejection

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 4, 7, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over MAFT (The MAFT Architecture for Distributed Fault Tolerance) in view of Official Notice, further in view of Lewis et al. (U.S. Patent No. 6,131,112).

As in claim 1, MAFT teaches of a computer system having a plurality of processor systems, each of the processor systems generating a plurality of error signals in response to different conditions on the processor systems, and a parallel transaction bus connected to each of the processor systems *(Fig. 1; page 399, left column, where the processor boards comprise an OC and AP; page 400, left column, paragraph 2, teaches of error signals; page 400, left column, paragraph 4, teaches of a parallel transaction bus connected to each of the processor boards)*, an error reporting network comprising:

a signal line, separate from the parallel transaction bus, and connected to each of the processor systems *(Fig. 1,2; page 400, left column, paragraph 1, inter-node message line serial broadcast link)*; and

each of the processor systems containing:

means for generating an error detection signal *(page 400, left column, paragraph 2, ERR)*;

means responsive to [one of the] control signals for generating an error notification signal and for communicating the error notification signal to each of the processor systems over said signal line *(page 400, left column, paragraph 2, BPC which is communicated to all nodes informing each of the error status of each node; the BPC message is inherently a response to a control signal)*; and

means responsive to one of the control signals for communicating the plurality of error signals to each of the processor systems serially over said signal line *(page 400, left column, paragraphs 1 and 2, where the OCs communicate the error messages via the serial broadcast link)*.

However, MAFT fails to teach of processor boards, a control means, and collecting and storing of error signals. The Examiner is taking Official Notice that it is well-known in the art to include separate processors on separate processor boards. Lewis et al. teaches of a control means responsive to an error detection signal for generating in sequence a plurality of control signals *(column 10 lines 4-5, generation of alarm signal; column 10 lines 4-64, where a sequence of a plurality of control signals comprises filtering, correlation, data storage, result display,*

corrective action, and/or additional alarm messages), and means responsive to one of the control signals for collecting and storing the plurality of error signals *(column 10 lines 45-49)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the processor boards as taught by Examiner taking Official Notice in the invention of MAFT. This would have been obvious because a processor board allows a processor to communicate with other computer system components. A processor board is extremely common and well-known in the art as a means for housing a processor and its necessary related components for proper operation in a computing system.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the control signal and storage means as taught by Lewis et al. in the invention of MAFT, including Official Notice. This would have been obvious because further processing of alarm signals and storing of such signals allows for better identification of a problem that exists within a distributed computing system.

As in claim 4, MAFT teaches a method of communicating an error status between processor systems of a computer system, each of the processor systems generating a plurality of error signals in response to different conditions on the processor systems, the computer system further having a parallel transaction bus connected to each of the processor systems *(Fig. 1; page 399, left column, where the processor boards comprise an OC and AP; page 400, left column, paragraph 2, teaches of error signals; page 400, left column, paragraph 4, teaches of a parallel transaction bus connected to each of the processor boards)*, and a signal line, separate from the parallel transaction bus, connected to each of the processor systems *(Fig. 1,2; page 400, left*

column, paragraph 1, inter-node message line serial broadcast link), each of the processor systems performing the steps of:

generating an error detection signal *(page 400, left column, paragraph 2, ERR)*;

generating an error notification signal and communicating the error notification signal to each of the processor systems over the signal line *(page 400, left column, paragraph 2, BPC which is communicated to all nodes informing each of the error status of each node; the BPC message is inherently a response to a control signal)*; and

communicating the plurality of error signals to each of the processor systems serially over the signal line *(page 400, left column, paragraphs 1 and 2, where the OCs communicate the error messages via the serial broadcast link)*.

However, MAFT fails to teach of processor boards, a control means, and collecting and storing of error signals. The Examiner is taking Official Notice that it is well-known in the art to include separate processors on separate processor boards. Lewis et al. teaches of a control means responsive to an error detection signal for generating in sequence a plurality of control signals *(column 10 lines 4-5, generation of alarm signal; column 10 lines 4-64, where a sequence of a plurality of control signals comprises filtering, correlation, data storage, result display, corrective action, and/or additional alarm messages)*, and means responsive to one of the control signals for collecting and storing the plurality of error signals *(column 10 lines 45-49)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the processor boards as taught by Examiner taking Official Notice in the invention of MAFT. This would have been obvious because a processor board allows a processor to communicate with other computer system components. A processor board is

extremely common and well-known in the art as a means for housing a processor and its necessary related components for proper operation in a computing system.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the control signal and storage means as taught by Lewis et al. in the invention of MAFT, including Official Notice. This would have been obvious because further processing of alarm signals and storing of such signals allows for better identification of a problem that exists within a distributed computing system.

As in claim 7, MAFT teaches a computer system, comprising:

a plurality of processor systems each generating a plurality of error signals in response to different conditions on said processor systems;

a parallel transaction bus connected to each of said processor systems; and

a signal line, separate from said parallel transaction bus, and connected to each of said processor systems *(Fig. 1; page 399, left column, where the processor boards comprise an OC and AP; page 400, left column, paragraph 2, teaches of error signals; page 400, left column, paragraph 4, teaches of a parallel transaction bus connected to each of the processor boards)*;

each of said processor systems containing:

means for generating an error detection signal *(page 400, left column, paragraph 2, ERR)*;

means responsive to one of the control signals for generating an error notification signal and for communicating the error notification signal to each of said processor systems over said

signal line *(page 400, left column, paragraph 2, BPC which is communicated to all nodes informing each of the error status of each node; the BPC message is inherently a response to a control signal)*; and

means responsive to one of the control signals for communicating the plurality of error signals to each of said processor systems serially over said signal line *(page 400, left column, paragraphs 1 and 2, where the OCs communicate the error messages via the serial broadcast link)*.

However, MAFT fails to teach of processor boards, a control means, and collecting and storing of error signals. The Examiner is taking Official Notice that it is well-known in the art to include separate processors on separate processor boards. Lewis et al. teaches of a control means responsive to an error detection signal for generating in sequence a plurality of control signals *(column 10 lines 4-5, generation of alarm signal; column 10 lines 4-64, where a sequence of a plurality of control signals comprises filtering, correlation, data storage, result display, corrective action, and/or additional alarm messages)*, and means responsive to one of the control signals for collecting and storing the plurality of error signals *(column 10 lines 45-49)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the processor boards as taught by Examiner taking Official Notice in the invention of MAFT. This would have been obvious because a processor board allows a processor to communicate with other computer system components. A processor board is extremely common and well-known in the art as a means for housing a processor and its necessary related components for proper operation in a computing system.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the control signal and storage means as taught by Lewis et al. in the invention of MAFT, including Official Notice. This would have been obvious because further processing of alarm signals and storing of such signals allows for better identification of a problem that exists within a distributed computing system.

As in claim 10, MAFT teaches a computer system, comprising a plurality of processor systems generating a plurality of error signals in response to different conditions on said processor systems;

a parallel transaction bus connected to each of said processor systems; and

a signal line, separate from said parallel transaction bus, connected to each of said processor systems *(Fig. 1; page 399, left column, where the processor boards comprise an OC and AP; page 400, left column, paragraph 2, teaches of error signals; page 400, left column, paragraph 4, teaches of a parallel transaction bus connected to each of the processor boards)*;

each of said processor boards communicating an error status between said processor systems by being programmed to:

generate an error detection signal *(page 400, left column, paragraph 2, ERR)*;

generate an error notification signal and communicate the error notification signal to each of said processor systems over said signal line *(page 400, left column, paragraph 2, BPC which is communicated to all nodes informing each of the error status of each node; the BPC message is inherently a response to a control signal)*; and

communicate the plurality of error signals to each of said processor systems serially over said signal line *(page 400, left column, paragraphs 1 and 2, where the OCs communicate the error messages via the serial broadcast link)*.

However, MAFT fails to teach of processor boards, a control means, and collecting and storing of error signals. The Examiner is taking Official Notice that it is well-known in the art to include separate processors on separate processor boards. Lewis et al. teaches of a control means responsive to an error detection signal for generating in sequence a plurality of control signals *(column 10 lines 4-5, generation of alarm signal; column 10 lines 4-64, where a sequence of a plurality of control signals comprises filtering, correlation, data storage, result display, corrective action, and/or additional alarm messages)*, and means responsive to one of the control signals for collecting and storing the plurality of error signals *(column 10 lines 45-49)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the processor boards as taught by Examiner taking Official Notice in the invention of MAFT. This would have been obvious because a processor board allows a processor to communicate with other computer system components. A processor board is extremely common and well-known in the art as a means for housing a processor and its necessary related components for proper operation in a computing system.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the control signal and storage means as taught by Lewis et al. in the invention of MAFT, including Official Notice. This would have been obvious because further processing of alarm signals and storing of such signals allows for better identification of a problem that exists within a distributed computing system.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2, 5, 8, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over MAFT, further in view of Official Notice, further in view of Lewis et al., further in view of Cho (U.S. PGPub 2002/0080930).

As in claims 2, 5, 8, and 11, the combined invention of MAFT, Official Notice, and Lewis et al. teaches the limitations of claims 1, 4, 7, and 10, respectively, including multiple processor boards. However, the combined invention of MAFT, Official Notice, and Lewis et al. fails to teach of the remainder of the claims limitations.

Cho teaches of storage means *(Fig. 2; paragraphs [0049] and [0056], memory 150)*;

further control means responsive to the error notification signal for generating in sequence a plurality of further control signals *(Fig. 2; paragraphs [0049]-[0054], where collection and storage of PSB signals inherently comprise a plurality of control signals)*;

means responsive to one of the further control signals for converting to parallel form and storing in said storage means as error information the plurality of error signals communicated

from each of the processor boards serially over said signal line *(paragraphs [0049] and [0056])*; and

means connected to said storage means for reading out the error information *(Fig. 2; paragraph [0049], buffer 160)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the storage means as taught by Cho in the combined invention of MAFT, Official Notice, and Lewis et al. This would have been obvious because storing of error information as taught by Cho allows for analysis of fault data while saving time and money in a computing system *(paragraph [0016])*.

* * *

3. Claims 3, 6, 9, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over MAFT, further in view of Official Notice, further in view of Lewis et al., further in view of Cho, further in view of Gerbehy et al. (U.S. Patent No. 5,410,542).

As in claims 3, 6, 9, and 12, the combined invention of MAFT, Official Notice, Lewis et al., and Cho teaches the limitations of claims 2, 5, 8, and 11, respectively. However, the combined invention of MAFT, Official Notice, Lewis et al., and Cho fails to teach the remainder of the limitations of the claims.

Gerbehy et al. teaches each of the processor boards is assigned a different slot number and said signal line is time division multiplexed between all of the processor boards, and said

control means being responsive to the slot number for controlling said means for communicating so as to communicate the plurality of error signals serially over said signal line within a predetermined time slot in relation to other ones of the processor boards *(column 8 lines 8-22)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the TDM as taught by Gerbehy et al. in the combined invention of MAFT, Official Notice, Lewis et al., and Cho. This would have been obvious because a TDM transmission path between processor boards increases the efficiency and reliability of a computer system *(column 1 lines 64-68)*.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

US PGPub 2003/0101385 Lee discloses processor boards and error management

US PGPub 2001/0008021 Ote et al. discloses fault logging

US PGPub 2004/0153870 Konz et al. discloses error signals in a distributed system

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PFC
9/18/2007

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER